REMARKS/ARGUMENTS

This Amendment is in response to the Office Action mailed November 9, 2007. Claims 1-2, 5-8, 11-14, and 16 were pending in the present application. This Amendment amends claims 1, 7, and 13; and cancels claims 14 and 16; leaving pending in the application claims 1-2, 5-8, and 11-13. Reconsideration of the rejected claims is respectfully requested.

I. Rejection under 35 U.S.C. §103

(a) *Gray, Becker*, and *Nguyen*

Claims 1, 2, 7-8, 13-14, and 16 are rejected under 35 U.S.C. 103(a) as being obvious over *Gray* (U.S. Pat. No. 6,816,923) in view of *Becker* (U.S. Pat. No. 6,950,884) and further in view of *Nguyen* (US 5,335,326). Applicants respectfully submit that these references do not teach or suggest each element of these claims.

Teachings of each of these references, and reasons why the combination of these references should not render these claims obvious, are discussed as of record and will not be reproduced herein. Instead, reasons for rejections set forth in the Office Action mailed November 9, 2007 will be discussed in turn.

As a reminder it is respectfully submitted that MPEP §2143 (Examples of Basic Requirements of a *Prima Facie* Case of Obviousness) that a conclusion of obviousness must be consistent with the proper "functional approach" to the determination of obviousness as laid down in *Graham*. As such, it is not sufficient merely to find elements of a claim in a number of different references used differently or in different systems, methods, or devices. There must be a clear articulation of the reason(s) why the claimed invention would have been obvious. Proper rationale for combining elements can include combining prior art elements according to known methods to yield predictable results, or some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention. It is respectfully submitted that the rejections in the Office Action do not meet such standards.

For example, the Office Action on pages 7-9 asserts that combining *Becker* with *Gray* would result in a "single circular buffer for buffering the transferring of data into each of Gray's device buffers...for the benefit of providing transfer of data and low delay flow coordination between two functional blocks". It is respectfully submitted that, even if for sake of argument it was obvious to combine the references, the combination would not arrive at the buffering approach of Applicants' claim 1.

As discussed previously, *Gray* teaches a direct memory access (DMA) system that includes a data reservoir for consolidating memory buffers for various devices (col. 2, lines 34-47; col. 3, line 64-col. 4, line 18). The Office Action alleges on page 7 that *Gray* teaches each of multiple data bursts being assigned to a respective buffer in response to a received memory access request as shown by Figures 2 and 3. Applicants refer to the text corresponding to these figures, in columns 11 and 12, where it is described that a data request is received when one or more channels of a device needs servicing (col. 11, lines 65-67). This allows arbitration to be performed one a per-device approach instead of per-channel approach. The only way this teaching can be construed to teach multiple bursts in response to a request is if the initial request concerning multiple channels for a device is considered the request, and the responses for each respective channel are considered bursts, or if the requests are for different devices and the responses for each device are considered different buffers, and each burst is contained in different buffers. If this rationale is used for citing the reference, then this rationale must also be considered when combining the references. There is no teaching of wrapping requests for data returned for multiple devices, or how one would utilize a wrapping memory access request in such a situation. Further, each burst is written to a separate buffer, and there is no teaching of concurrently storing information for a beginning and ending of a request in a single common buffer, which provides the ability to cache data needed for the end of the request without the need to obtain another burst for the end of the request.

The Office Action asserts on pages 8 and 9 that the wrapping and sub-buffer aspects are remedied by combining *Gray* with *Becker*. *Becker* teaches using "cyclic memories," wherein read and write access between two processors takes place in rising or falling memory block order (col. 8, line 65-col. 9, line 6). For example, when the last block of one control information

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The Office Action asserts on pages 8 and 9 that the wrapping and sub-buffer aspects are remedied by combining *Gray* with *Becker*. *Becker* teaches using "cyclic memories," wherein read and write access between two processors takes place in rising or falling memory block order (col. 8, line 65-col. 9, line 6). For example, when the last block of one control information

memory is reached, the first block is automatically written to as the next memory block (col. 8, line 65-col. 9, line 6). Here, the Office Action asserts that *Becker* teaches data for the beginning and end being assigned to respective sub-buffers (OA page 8). It is respectfully submitted that if an attempt is made to read *Becker* as closely as possible to Applicants' claim 1, *Becker* can either be construed to:

(1) write portions of a request to sub-buffers of a single buffer, where the single buffer contains all information for the request, or

(2) require multiple buffers (where each of the sub-buffers of *Becker* are considered a buffer), but not write different portions of the request to a single buffer.

Applicants' claim 1 addresses the case where "a wrapping memory access request requires multiple buffers" and "data required for each of a beginning and an end of the wrapping memory access request are assigned to respective sub-buffers of a single respective buffer." *Becker* does not teach such a situation. The Office Action states that it is construing (sub_1, sub_2, sub_3, ...) as sub-buffers of a single respective buffer (the single circular buffer) (OA p. 8). If this is the case, then this does not address the case of a request that requires multiple buffers, and how to wrap and store data across those multiple buffers. The approach of *Becker* is all within a single buffer.

If the Office Action attempts to then say that such an approach could be extrapolated to multiple buffers instead of multiple sub-buffers, then such a reading still would not meet the limitations of the claims, as such an approach would then store circularly across the multiple buffers, but there would be no teaching of suggestion of storing a beginning and end in a portion of one of these buffers, as the approach would instead store circularly but in separate buffers. *Becker* teaches wrapping within a single buffer, but does not teach wrapping among multiple buffers, which further involves concurrently storing separate portions of a request in a single buffer.

Combining such teaching with Gray, if there were motivation to do so, would at best store information for each device in a single wrapping buffer, but would not concurrently store data from a single data burst in respective sub-buffers, where the data required for the end of the

wrapping memory request is cached in the respective sub-buffer until needed for transfer in response to the wrapping memory access request by the memory interface.

Accordingly, it is respectfully submitted that this portion of the rejection does not arrive at the respective element of the memory controller of claim 1.

The Office Action also combines *Nguyen* with these references in an attempt to show the use of a pointer as recited in Applicants' claim 1. *Nguyen* teaches a bus-to-bus interface including a central buffer means including first and second FIFO devices, utilizing a pointer means to traverse a circular queue in the FIFO devices slot by slot (col. 1, line 59-col. 2, line 49). Even if for sake of argument it would have been obvious to combine the pointer of *Nguyen* with the combination set forth above, the pointer (*Nguyen*) would still at best keep track of the next sub-buffer in the single circular buffer (*Becker*) for each device (*Gray*). The recited references cannot in any way be combined to show that

> for a wrapping memory access request **requiring multiple buffers, data required for each of a beginning and an end of the wrapping memory access request are assigned to respective sub-buffers of a single respective buffer** by the control logic, the beginning and end data for the memory access request **being stored concurrently from a single data burst in the respective sub-buffers** by the memory interface, the storing of the beginning and end data in a single buffer avoiding the need for an additional data burst to obtain the end data, **the data required for the end of the wrapping memory request being cached in the respective sub-buffer until needed for transfer in response to the wrapping memory access request**

(*emphasis added*). The combination would not meet these limitations, even given the broadest possible interpretation as set forth above.

Further, Applicants' claim 1 has further been amended to clarify that each of the plurality of buffers is sized to store a data burst for a memory access request, and each of the plurality of buffers further includes a plurality of sub-buffers each sized to store a data beat of the data burst stored in the corresponding buffer. Such limitations even further limit the ability to read the references as broadly as is set forth above.

For at least these reasons, the combination of *Gray*, *Becker*, and *Nguyen* fails to teach or suggest each element of Applicants' claim 1, such that these references cannot render obvious

Applicants' claim 1 or the claims that depend therefrom. Independent claims 7 and 13 recite limitations that similarly are not rendered obvious by these references for reasons including those cited above. Applicants therefore respectfully request that the rejection with respect to claims 1, 2, 7-8, 13-14, and 16 be withdrawn.

(b) *Gray, Becker, Nguyen,* and *Kuronuma*

Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being obvious over *Gray, Becker*, and *Nguyen*, and further in view of *Kuronuma* (U.S. Pat. No. 6,859,848). Claims 5 and 11 depend from claims 1 and 7, respectively, which are not rendered obvious by *Gray, Becker*, and *Nguyen* as discussed above. *Kuronuma* does not make up for the deficiencies in *Gray, Becker*, and *Nguyen* with respect to these claims. *Kuronuma* teaches a memory control system for sequentially accessing an arbitrary address in an SDRAM circuit (col. 4, lines 22-25), and is cited as teaching sequential access to an SDRAM (OA page 10). *Kuronuma* does not, however, teach or suggest a memory controller with control logic assigning different portions of a single request from a single device to multiple buffers as well as beginning and end portions to different sub-buffers of a single buffer, and recording a pointer so that the control logic can come back to the single buffer in order to obtain the end portion of the data without requiring an additional data burst. As such, *Kuronuma* cannot render obvious claims 1 and 7, or dependent claims 5 and 11, alone or in any combination with *Gray, Becker*, and *Nguyen.* Applicants therefore respectfully request that the rejection with respect to claims 5 and 11 be withdrawn.

(c) *Gray, Becker, Nguyen* and *Microsoft*

Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being obvious over *Gray, Becker*, and *Nguyen*, and further in view of *Microsoft* ("Microsoft Computer Dictionary", 2002 p. 469). Claims 6 and 12 depend from claims 1 and 7, respectively, which are not rendered obvious by *Gray, Becker*, and *Nguyen* as discussed above. *Microsoft* does not make up for the deficiencies in *Gray, Becker*, and *Nguyen* with respect to these claims. *Microsoft* is cited as teaching SDRAM as a common type of RAM (OA page 11). *Microsoft* does not, however, teach or suggest a memory controller with control logic assigning different portions of a single request

from a single device to multiple buffers as well as beginning and end portions to different sub-buffers of a single buffer, and recording a pointer so that the control logic can come back to the single buffer in order to obtain the end portion of the data without requiring an additional data burst. As such, *Microsoft* cannot render obvious claims 1 and 7, or dependent claims 6 and 12, alone or in any combination with *Gray, Becker*, and *Nguyen.* Applicants therefore respectfully request that the rejection with respect to claims 6 and 12 be withdrawn.

II. Amendment to the Claims

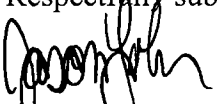
Unless otherwise specified or addressed in the remarks section, amendments to the claims are made for purposes of clarity, and are not intended to alter the scope of the claims or limit any equivalents thereof. The amendments are supported by the specification and do not add new matter.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 925-472-5000.

Respectfully submitted,



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